an initial step of forming a first epitaxial region 11 of the N⁻ type, followed by a masking, implanting, and P-dopant diffusing step to form a buried layer 12 of the isolation well.

Paragraph beginning at line 6 of page 3 has been amended as follows:

In particular, the buried layer 12, additionally to providing part of the buried insulator for the drive circuitry or region LV, provides here part of the base region of the NPN power component or region HV.

Paragraph beginning at line 9 of page 3 has been amended as follows:

A subsequent masking, implanting, and N-dopant diffusing step, carried out at the buried layer 12, will bulk delimit the N-type regions 2 intended to contain various circuitry components, as described in connection with the prior art shown in Figure 1.

Paragraph beginning at line 12 of page 3 has been amended as follows:

The buried layer 12, besides providing the emitter for the NPN power component in the region HV, also functions as a buried collector and buried drain for the NPN and VDMOS signal components, respectively, in the region LV.

Paragraph beginning at line 15 of page 3 has been amended as follows:

An additional epitaxial region 3 is necessary to provide N-type isolated wells IS. These wells are fully delimited with an additional masking, implanting, and P-type diffusing step to form the isolation regions 4 in the epitaxial region 3 and ensure electrical continuity to the buried region 12.

Paragraph beginning at line 1 of page 4 has been amended as follows:

Note should be taken that the above conventional isolation well structures IS closely resemble each other. The only differences to be seen are in the substrate, of the P type or the N type, and the integration of the region 12 with VIPower technology.

Paragraph beginning at line 8 of page 5 has been amended as follows:

The features and advantages of the integrated device with an isolation structure, according to this invention, will be apparent from the following description of embodiments thereof, given by way of non-limitative examples with reference to the accompanying drawings, wherein:

Figure 1 is a schematic cross-sectional view of an integrated device with a junction type of isolation structure, according to the prior art;

Figure 2 is a schematic cross-sectional view of an integrated device with a junction type of isolation structure, as formed with a conventional low-power technology;

Figure 3 is a schematic cross-sectional view of an integrated device with a junction type of isolation structure, as formed with a conventional VIPower technology;

Figure 4 is a schematic cross-sectional view of an integrated device with a trench type of isolation structure, according to the invention;

Figures 5 to 5e show successive process steps for fabricating the integrated device with a trench type of isolation structure, according to the invention;

Figure 6 is a schematic cross-sectional view of another embodiment of an integrated device formed in accordance with the present invention;

Figure 7 is a schematic cross-sectional view of another embodiment of an integrated device formed in accordance with the present invention;

Figure 8 is a schematic cross-sectional view of another embodiment of an integrated device formed in accordance with the present invention;

Figure 9 is a schematic cross-sectional view of another embodiment of an integrated device formed in accordance with the present invention; and

Figure 10 is a schematic cross-sectional view of another embodiment of an integrated device formed in accordance with the present invention.

In the Claims:

Please cancel claim 18.

Please amend claims 1, 4, and 17 to read as follows:

1. (Amended) An integrated device, comprising: a substrate wherein a buried layer and an epitaxial region have been formed, and an isolation structure adapted to define a plurality of isolation wells for integrating the components of the integrated device therein, said isolation structure comprises plural dielectrically insulated trenches, each trench having an open bottom and each trench filled with a conductive material to form a contact region that is in direct contact with one of the substrate and buried layer.

4. (Amended) The integrated device of claim 2 wherein the plurality of trenches are in contact with said buried layer and are located at each edge of each isolation well.

17. (Amended) An isolation trench structure, comprising:

a substrate having a buried layer and an epitaxial region formed therein;

a plurality of isolation wells formed in the substrate; and

a dielectrically insulated trench formed between each of the isolation wells and located at the edges of the isolation wells, each trench having an open bottom and each trench comprising a central contact region surrounded by insulating dielectric regions, each central contact region formed of electrically conductive material that is in direct contact with the buried layer.

REMARKS

Claims 1-8, 17, 19, and 20 are presented for further examination. Claim 18 has been canceled. Claims 1, 4, and 17 have been amended.

In the Office Action mailed May 31, 2002, the Examiner objected to the title and requested a new title that was more descriptive. Applicant has so amended the title. In addition, the drawings were objected to because the reference character "1" has been used to designate both the substrate and the buried region. Applicant is submitting herewith proposed drawing changes to Figures 3, 9, and 10 showing in red the changes to be made therein. Applicant respectfully requests that the proposed drawing changes be approved and entered in the application. Formal drawings will be provided upon allowance of the claims.

Claim 4 was rejected under 35 U.S.C. § 112, second paragraph, as indefinite. Applicant has amended claim 4 to overcome the indefiniteness. Claims 1-8, 17, 18, and 20 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,665,633 ("Meyer"). Claim 19 was rejected under 35 U.S.C. § 103(a) as obvious over Meyer.

Applicant respectfully disagrees with the bases for the rejections and requests reconsideration and further examination of the claims.

The present invention is directed to a trench structure that provides isolation in integrated devices. A trench is placed in contact with a buried oxide layer on each side of an isolation well to reduce the dimensions of the isolation well and enhance the isolation conditions. In accordance with the invention, the trenches provide for lateral insulation of integrated components by insulating the wells where they are fabricated. Moreover, such trenches are to be considered as part of the active area of the integrated elements because they allow a current flow from the silicon bulk toward the surface of the integrated circuit. Thus, the trenches are both insulating and active elements in the integrated device. This is accomplished because of the open bottom of the trench and the use of electrically conductive material as a contact region inside the trench.

U.S. Patent No. 5,665,633, Meyer, is directed to a process for forming a semiconductor device having field isolation. Meyer teaches shallow trenches, simply integrated near each other in order to constitute a type of a "comb" that extends as far as the desired field region. After lateral wall oxidation, the trenches are always distinct one to the other by gap silicon regions. Thus, Meyer teaches a plurality of wide and narrow field regions provided on the same wafer, the minimum width thereof corresponding to the minimum width of the trench and the edge of a generic active area of an integrated element being defined by a trench. Meyer does not teach the trenches having open bottoms to provide an active area within the insulating trench.

Turning to the claims, claim 1 is directed to an integrated device that comprises a substrate wherein a buried layer and an epitaxial region have been formed, and an isolation structure adapted to define a plurality of isolation wells for integrating the components of the integrated device therein, the isolation structure comprising plural dielectrically insulated trenches, each trench having an open bottom and each trench filled with a conductive material to

form a contact region that is in direct contact with one of the substrate and buried layer. As discussed above, nowhere does Meyer teach or suggest a trench having an open bottom and filled with conductive material that is in direct contact with one of the substrate and the buried layer. Rather, in Meyer, the trenches are lined with insulating material (136) that electrically isolates the trench from the underlying substrate. Clearly, Meyer teaches away from the embodiment recited in claim 1. Applicant respectfully submits that claim 1, and dependent claims 2-8 are clearly in condition for allowance.

Independent claim 17 is directed to an isolation trench structure that comprises a substrate having a buried layer and an epitaxial region formed therein; a plurality of isolation wells formed in the substrate; and a dielectrically insulated trench formed between each of the isolation wells and located at the edges of the isolation wells, each trench having an open bottom and each trench comprising a central contact region surrounded by insulating dielectric regions, each central contract region formed of electrically conductive material that is in direct contact with the buried layer. As discussed above with respect to claim 1, Meyer teaches insulating each trench from the underlying buried layer, which is inapposite to the present claimed invention. Consequently, applicant respectfully submits that claim 17, as well as dependent claims 19 and 20 are allowable over the reference cited and applied by the Examiner.

In view of the foregoing, applicant respectfully submits that all of the claims remaining in this application are in condition for allowance. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicant's undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of the application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version With Markings to Show Changes Made**."

Respectfully submitted,

Salvatore Leonardi

SEED Intellectual Property Law Group PLLC

E. Russell Tarleton
Registration No. 31,800

ERT:aep

Enclosure:
Postcard
Request for Drawing Change

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031